THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

BONG-JOON LEE, et al.

Application No. NEW

Filed: Herewith

For: **DATA SAMPLING METHOD AND APPARATUS WITH ALTERNATING EDGE SAMPLING PHASE DETECTION FOR LOOP CHARACTERISTIC STABILIZATION**

Group Art Unit: Unknown

Examiner: Unknown

INFORMATION DISCLOSURE STATEMENT

400 Montgomery Street
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San Francisco, CA 94104
(415) 433-2250

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant submits herewith patents, publications or other information [attached hereto and listed on the attached Form PTO-1449 (modified)] of which he is aware, which he believes may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

This Information Disclosure Statement:

(a) [] accompanies the new patent application submitted herewith. 37 CFR § 1.97(a).

(b) [X] is filed within three months after the filing date of the application or within three months after the date of entry of the national stage of a PCT application as set forth in 37 CFR § 1.491.

(c) [] as far as is known to the undersigned, is filed before the mailing date of a first Office Action on the merits.

(d) [] is filed after the first office action and more than three months after the application's filing date or PCT national stage date of entry filing but, as far as is known to the undersigned, prior to the mailing date of either a final rejection or a notice of allowance, whichever occurs first, and is accompanied by either the fee ($180) set forth in 37 CFR § 1.17(p) **or** a certification as specified in 37 CFR § 1.97(e), as checked below.

(e) [] is filed after the mailing date of either a final rejection or a notice of allowance, whichever occurred first, and the Issue Fee has not been paid, and is accompanied by the fee ($130) set forth in 37 CFR § 1.17(i)(1) and a certification as specified in 37 CFR § 1.97(e), as checked below. This document is to be considered as a petition requesting consideration of the information disclosure statement.

[If either of boxes (d) or (e) are checked above, the following "certification" under 37 CFR § 1.97(e) may need to be completed.] The undersigned certifies that:

(f) [] Each item of information contained in the information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

(g) [] No item of information contained in this information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this information disclosure statement.

A list of the patent(s) or publication(s) is set forth on the attached Form PTO-1449 (Modified).

A copy of the items on PTO-1449 (Modified) is supplied herewith:

(h) [X] each (i) [] none (j) [] only those listed below:

Those patent(s) or publication(s) which are marked with an asterisk (*) in the attached form PTO-1449 (Modified) are not supplied because they were previously cited by or submitted to the Office in a prior application

no. , filed and relied upon in this application for an earlier filing date under 35 U.S.C. § 120.

A concise explanation of relevance of the items listed on form PTO-1449 (Modified) is:

(k) [X] not given

(l) [] given for each listed item

(m) [] given for only non-English language listed item(s) [Required]

(n) [] is in the form of an English language copy of a Search Report from a foreign patent office, issued in a counterpart application, which refers to the relevant portions of the references [copy attached].

The Examiner is reminded that a "concise explanation of the relevance" of the submitted items "may be nothing more than identification of the particular figure or paragraph of the patent or publication which has some relation to the claimed invention," MPEP § 609.

While the information and references disclosed in this Information Disclosure Statement may be "material" pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR § 1.56(a) exists. It is submitted that the Information Disclosure Statement is in compliance with 37 CFR § 1.98 and MPEP § 609 and the Examiner is respectfully requested to consider the listed references.

[] The Commissioner is hereby authorized to charge our Deposit Account No. **50-1697** for any fees required in connection with the filing of this Information Disclosure Statement. **A duplicate copy of this Notice is enclosed for this purpose.**

Respectfully submitted,

Dated: 8/12/03 By _____

Alfred A. Equitz
Registration No. 30,922
Tel. No. 415/433-2250

Our File: SII-2510 [SMIG0155]

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-2510 [SMIG0155]	Appln. No. NEW
	Applicant(s) BONG-JOON LEE, et al.	
	Filing Date Herewith	Group Unknown

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
	AA						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	AB							

OTHER DOCUMENTS

	AC	Savoj, J. et al., ***"A 10-Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector"*** IEEE Journal of Solid-State Circuits, Vol. 36, No. 5, May 2001, pages 761-767.
	AD	Lee, Sang-Hyun, et al., ***"A 5Gb/s 0.25μm CMOS Jitter-Tolerant Variable-Interval Oversampling Clock/Data Recovery Circuit,"*** 2002 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pages 256-257 and 465 (February 2002).
	AE	Moon, Yongsam, et al., ***"A 0.6 – 2.5Gbaud CMOS Tracked 3x Oversampling Transceiver with Dead-Zone Phase Detection for Robust Clock/Data Recovery,"*** 2001 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pages 212-213 and 448 (February 2001).
	AF	Green, M, et al., ***"OC-192 Transmitter in Standard 0.18μm CMOS,"*** 2002 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pages 248-249 (February 2002).
	AG	Fiedler, A., et al., ***"A 1.0625Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis,"*** 1997 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pages 238-239 (February 1997).
	AH	Larsson, Patrik, ***"A 2-1600-MHz CMOS Clock Recovery PLL with Low-Vdd Capability,"*** IEEE Journal of Solid-State Circuits, Vol. 34, No. 12, December 1999, pages 1951-1960.

Examiner	Date Considered

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.